Power Dissipation analysis of Conventional CMOS and Adiabatic CMOS circuits.
Sakshi Goyal*, Gurvinder Singh*, Pushpinder Sharma*
*Student **Assistant Professor
Electronics and Communication Department, Baba Farid Group of Institutes,
Deon, Bathinda, Punjab, India

Abstract: In recent years, low power circuit design has been an important issue in VLSI design areas. If the power consumption is less, then the amount of power dissipation is also less. Energy recovery adiabatic logic circuit is a low power design solution. Adiabatic circuits are those circuits which work on the principle of adiabatic charging and discharging. These circuits recycle the energy from output nodes instead of discharging it to ground. This paper presents the detail survey of relevant literature on adiabatic logic circuits published in the standard journals and database. There are many low power design techniques at different abstraction levels of digital system design. This paper gives literature survey on low power design techniques and justifies the need of energy recovery adiabatic technique over conventional CMOS.

Keywords: power dissipation; adiabatic switching; ECRL; PFAL; adiabatic circuits

I. Introduction

Technology has been grown to the large extent in the existing era. The most important issue in electronic devices especially for those which are portable is power and energy efficiency [1]. The objective of this paper is to provide low power solution to the VLSI designers. In conventional or traditional CMOS circuits, power dissipation can be minimized by reducing the supply voltage, node capacitance, and switching activity to a certain extent, but a technique called as adiabatic computing has been appeared proved to be a practical solution in the design of low power VLSI systems. The main causes of power dissipation in CMOS circuits is due to the charging and discharging of the node capacitances of the circuits, present both as a load and as parasitic. Such part of the total power dissipated by a circuit is called dynamic power [1-15]. In order to reduce the dynamic power, adiabatic switching has been proposed in the last years. In this approach, the charging and discharging process of the node capacitances is carried out in such a way that a small amount of energy is wasted and a recycling of the energy stored on the capacitors is done.

II. Power dissipation in CMOS circuits

Dissipated Energy is defined as the difference between the energy that the circuit needs to load the output capacitance, and the energy that the circuit gives back to the power supply during the recovery phase [2]. Power dissipation in digital CMOS circuits can be classified into two types:

- Dynamic power dissipation
- Static power dissipation.

Static power dissipation depends on the logic states of the circuit and Dynamic power dissipation is due to high-to-low and low-to-high signal switching in circuits[9][6][2]. The average power dissipation in a digital CMOS circuit is given by the following equation:

\[ P_{avg} = P_{sw} + P_{sc} + P_{leak} + P_{static} \]  \hspace{1cm} (1)

Where, \( P_{sw} \) is the capacitive switching power dissipation, \( P_{sc} \) is the short-circuit power dissipation, \( P_{leak} \) is the power dissipation due to leakage currents and \( P_{static} \) is the static power dissipation due to non-leakage static currents.

1) Static power dissipation: Static power dissipation can however result from degenerated voltage levels at the inputs to static gates. Bus contention, signal conflicts due to multiple drivers, leakage current drawn continuously from the power supply also result in static power dissipation.

2) Dynamic Power Dissipation: Dynamic power dissipation is caused by charging and discharging of capacitances. The charging process draws energy equal to \( C_{VDD} \) from the power supply. Half of this is dissipated immediately in the PMOS transistors and the interconnect, while the other half is stored on the load capacitance [9]. The energy stored in the capacitor gets dissipated across the NMOS and the interconnect. In summary, every time a capacitive node switches from ground to \( VDD \) (and back to ground), energy of \( C_{VDD} \) is consumed. Depends on the switching activity:

\[ P_{dyn} = aC_{VDD}f \]  \hspace{1cm} (2)

3) Short Circuit Power Dissipation: It is caused by the flow of short circuit current between supply and ground during switching or transition in signal values when NMOS and PMOS both are on[2][7].

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III. Need and Significance of low power dissipation

In modern circuit design, Low power is the major consideration. From past few years, several effective power management design techniques have been developed that include lowering of supply voltage.

- Mobile computing devices such as laptop computers, personal digital assistants, mobile gaming console, portable mp3 players, portable DVD players, photo storage and reviewing devices and cellular phones among the other are getting increased popularity.
- In the absence of low power design technique, portable and hand handheld products would suffer from very short battery life, while packaging and cooling would be very difficult.
- To protect the device from thermal breakdown this also results in increase of total area of the device.
- In addition reliability is also affected by power consumption.
- Finally, from environmental point of view, lower the power dissipation of the product lesser is the electricity consumed and lower is the impact on global environment.

IV. Adiabatic Circuits

The term “adiabatic” meant as a thermodynamic process in which there is no exchange of energy with the environment, and hence no energy or power dissipation occurs. Adiabatic technology is basically used to reduce the power or energy dissipation during the switching process and further recycle some of the energy by recycling it from the load capacitance [6][14].

- For recycling, the adiabatic circuit uses the principle of Constant current source power supply
- For reducing dissipation it uses the principle of Trapezoidal or sinusoidal power supply voltage.

Adiabatic logic works on the principal of reversible logics. Reversible logic means when a system erases a bit of information, it dissipates heat and today’s computers erase a bit of information every time they perform a logic operation. These are called irreversible logics [8]. And in contrast to it, the logic operations that do not erase information these are called reversible logics. Today most research has focused on building adiabatic logic out of CMOS. However, current CMOS technology, though fairly energy efficient compared to similar technologies, dissipate energy as heat, mostly when switching [4][6]. To reduce this there are two fundamental rules:

- Never turn on a transistor when there is voltage difference between drain and source.
- Never turn off a transistor that has current flowing through it [2].

As the second rule states that the transistor must not be turned off when there is current flowing through it, reason behind this is that the transistors are not perfect switches. The change from one state to another is directly proportional to the speed at which the gate voltage changes.[2]

Figure 1 shows the Charging and Discharging in CMOS System. Figure 2 shows the Charging and Discharging in Adiabatic System. In figure F functional block use PMOS transistor and F’ use NMOS transistor [4][7][9].

Figure 1: Charging and Discharging in CMOS System

Figure 2: Charging and Discharging in Adiabatic system
V. Adiabatic Circuit Types

In literature, today various kinds of adiabatic circuits proposed [1] all of them can be grouped into two fundamental classes:

- Fully Adiabatic Circuit
- Partially energy recovery Adiabatic Circuit (Quasi)

Popular Partially Adiabatic families include the following:
- Efficient Charge Recovery Logic (ECRL).
- 2N-2N2P Adiabatic Logic.
- Positive Feedback Adiabatic Logic (PFAL).
- NMOS Energy Recovery Logic (NERL).
- Clocked Adiabatic Logic (CAL).
- True Single-Phase Adiabatic Logic (TSEL).
- Source-coupled Adiabatic Logic (SCAL).

Some Fully adiabatic logic families include:
- Pass Transistor Adiabatic Logic (PAL).
- Split-Rail Charge Recovery Logic (SCRL).

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Fully Adiabatic</th>
<th>Partially Energy Adiabatic</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>All charge on the load capacitance is recovered by the power supply.</td>
<td>Some charge is allowed to be transferred to the ground.</td>
</tr>
<tr>
<td>2</td>
<td>More complex architecture.</td>
<td>Simpler architecture.</td>
</tr>
<tr>
<td>3</td>
<td>Lose energy due to leakage current through non ideal switches.</td>
<td>Energy loss is directly proportional to the capacitance driven and square of threshold voltage.</td>
</tr>
<tr>
<td>4</td>
<td>Face a lot of problems with respect to the operating speed and the inputs power clock synchronization.</td>
<td>It does not face much problem with respect to the operating speed and the inputs power clock synchronization.</td>
</tr>
</tbody>
</table>

VI. Efficient Charge Recovery Logic

Figure 3 shows the Efficient Charge Recovery Logic (ECRL) and was proposed by Moon and Jeong. It uses two cross-coupled PMOS transistors and two NMOS transistors in the N-functional blocks for the ECRL adiabatic logic block [5].

![Figure 3: Ecrl Inverter](image)

VI. Positive Feedback Adiabatic Logic

The partial energy recovery circuit structure named Positive Feedback Adiabatic Logic (PFAL) [15] has been used, since it shows the lowest energy consumption if compared to other similar families, and a good robustness against technological parameter variations. It is a dual-rail circuit with partial energy recovery. The general schematic of the PFAL gate is shown in Figure 4.3. The core of all the PFAL gates is an adiabatic amplifier, a latch made by the two PMOS M1-M2 and two NMOS M3-M4, that avoids a logic level degradation on the output nodes out and /out. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs [1].
A few research papers are available on IEEE, IET, ACS and DELNET database which report the results of various experiments performed on adiabatic benchmark circuits. In this section, the literature survey of these papers is presented.  
Cutilaru, M. et al. (2013) proposes a single-phase partially-adiabatic logic family and compares its energy characteristics with other adiabatic families by simulating a full-adder (FA) and an 8-bit carry-lookahead adder (CLA)[13]. Full-adder simulation results show that the proposed family uses up to 79% less energy compared to its CMOS equivalent and up to 67% less than other adiabatic implementations. The proposed 8-bit adiabatic CLA performs at least as well as the next best implementation while using a single phase clock instead of a four-phase clock.

M. C Knapp, et al studied the performance of 4X4 bit adiabatic multiplier against that of conventional CMOS [19] and showed that adiabatic circuits have large latencies (i.e. output lags three to five phase delays after the input signal) due to the dynamic nature of their gates. They observed that adiabatic memory elements had a latency of one clock cycle and hence they concluded that adiabatic technology was more effective for low speed, combinational circuits.

M. Alioto, et al evaluated the performance of adiabatic gates and their analysis indicated that additional reversible logic circuit required in full-adiabatic circuit increased power dissipation and complexity of the adiabatic circuit [17]. These were among the first few researchers who emphasized on quasi-adiabatic logic styles for their practical advantages like less complex logic structure, less silicon area at the price of additional non adiabatic loss. Their experiments indicated that 2N-2P and 2N-2N2P do not perform well at the gate level.

The conclusion that we can draw from the above literature survey is that adiabatic circuits dissipates less power than conventional CMOS circuits. Also, Full-adiabatic circuits like SCRL, RERL go long way towards achieving adiabatic operation. But they make the circuit complex and offers low throughput. In contrast to this Quasi-adiabatic logic styles viz. 2N2P, 2N-2N2P, and PAL which use cross coupled PMOS transistors are more practical circuits as these reduce the complexity of the circuit at the cost of little non-adiabatic loss. It appears that there is a possibility of improving the performance of such quasi-adiabatic circuits, in terms of energy dissipation and delay, by using circuit techniques.

References


